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DATA SHEET

74F225
16X5 asynchronous FIFO (3-State)

Product specification

1992 Jun 15

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

16 × 5 asynchronous FIFO (3-State) 74F225

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16 words of 5 bits
- DC to 25MHz data rate
- 3–State outputs
- Cascadable in word–width and depth direction

DESCRIPTION

This 80–bit active element First–In–First–Out (FIFO) is a monolithic Schottky–clamped transistor–transistor logic (STTL) array organized as 16–words of 5–bits each. A memory system using the 'F225 can be easily expanded in multiples of 16–words of 5–bits as shown in Figure 1. The 3–State outputs controlled by a single enable input ($\overline{OE}$) make bus connection and multiplexing simple. The 'F225 processes data in a parallel format at any desired clock rate from DC to 25MHz. Status of the 'F225 is provided by three outputs, Input Ready (IR), Unload Clock Output (UNCPOUT) and Output Ready (OR). The data outputs are non–inverting with respect to the data inputs and are disabled when the $\overline{OE}$ input is High. When $\overline{OE}$ is Low, the data outputs are enabled to function as totem–pole outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F225	25MHz	65mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20–pin plastic DIP	N74F225N	SOT146-1
20–pin plastic SOL	N74F225D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CPA, CPB	Load clock A and load clock B inputs	1.0/0.033	20µA/20µA
D0 – D4	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input (active–Low)	1.0/0.033	20µA/20µA
UNCPIN	Unload clock input	1.0/0.033	20µA/20µA
$\overline{MR}$	Master reset input (active–Low)	1.0/0.033	20µA/20µA
IR	Input ready output	50/33	1.0mA/20mA
UNCPOUT	Unload clock output (active–Low)	50/33	1.0mA/20mA
Q0 – Q4	Data outputs	150/40	3.0mA/24mA
OR	Output ready output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

RESET MODE

A High–to–Low transition on the Master Reset ($\overline{MR}$) input invalidates all data stored in the FIFO by clearing the control logic and setting OR Low. This High–to–Low transition on the $\overline{MR}$ input does not effect the data outputs but since OR is driven Low, it signifies invalid data on the outputs.

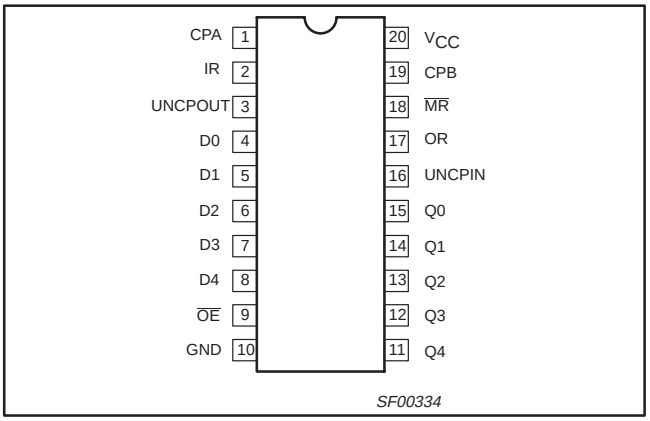
WRITE MODE

Data may be written into the array on the Low–to–High transition of either load clock (CPA or CPB) input. When writing data into the FIFO, one of the load clock inputs must be held High while the other strobes data into the FIFO. This arrangement allows either load clock to function as an inhibit for the other. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is High whenever the FIFO is available to accept new data. The unload clock output (UNCPOUT) also monitors the last word location. This output generates a Low–logic–level pulse (synchronized to the internal clock pulse) when the last word location is vacant

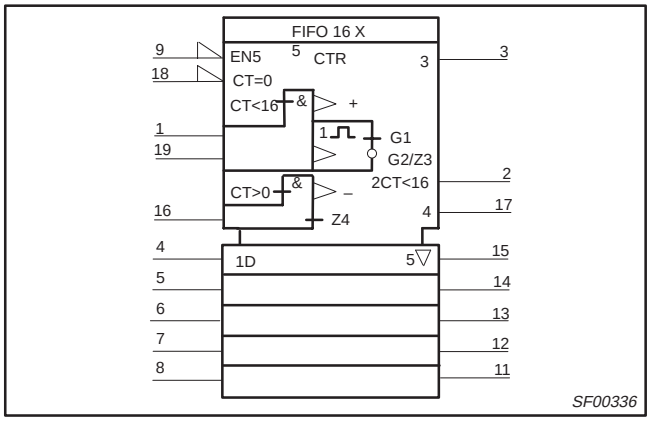
READ MODE

The Output Ready (OR) output is High when valid data is present on the data outputs. Data in the array is shifted on the Low–to–High transition of the Unload Clock Input (UNCPIN). In order for Output Ready (OR) to go High, Unload Clock Input (UNCPIN) must also be High.

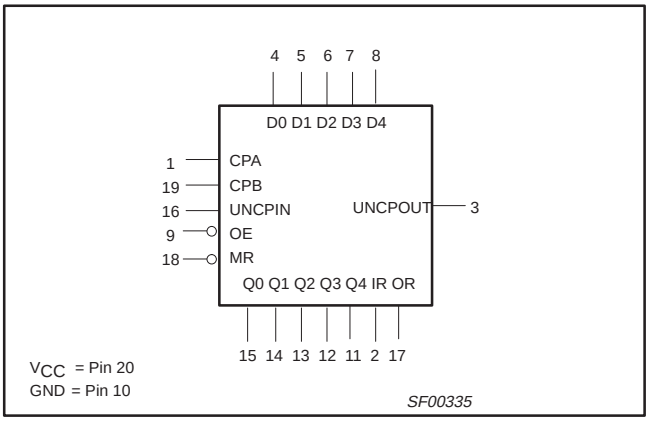
PIN CONFIGURATION



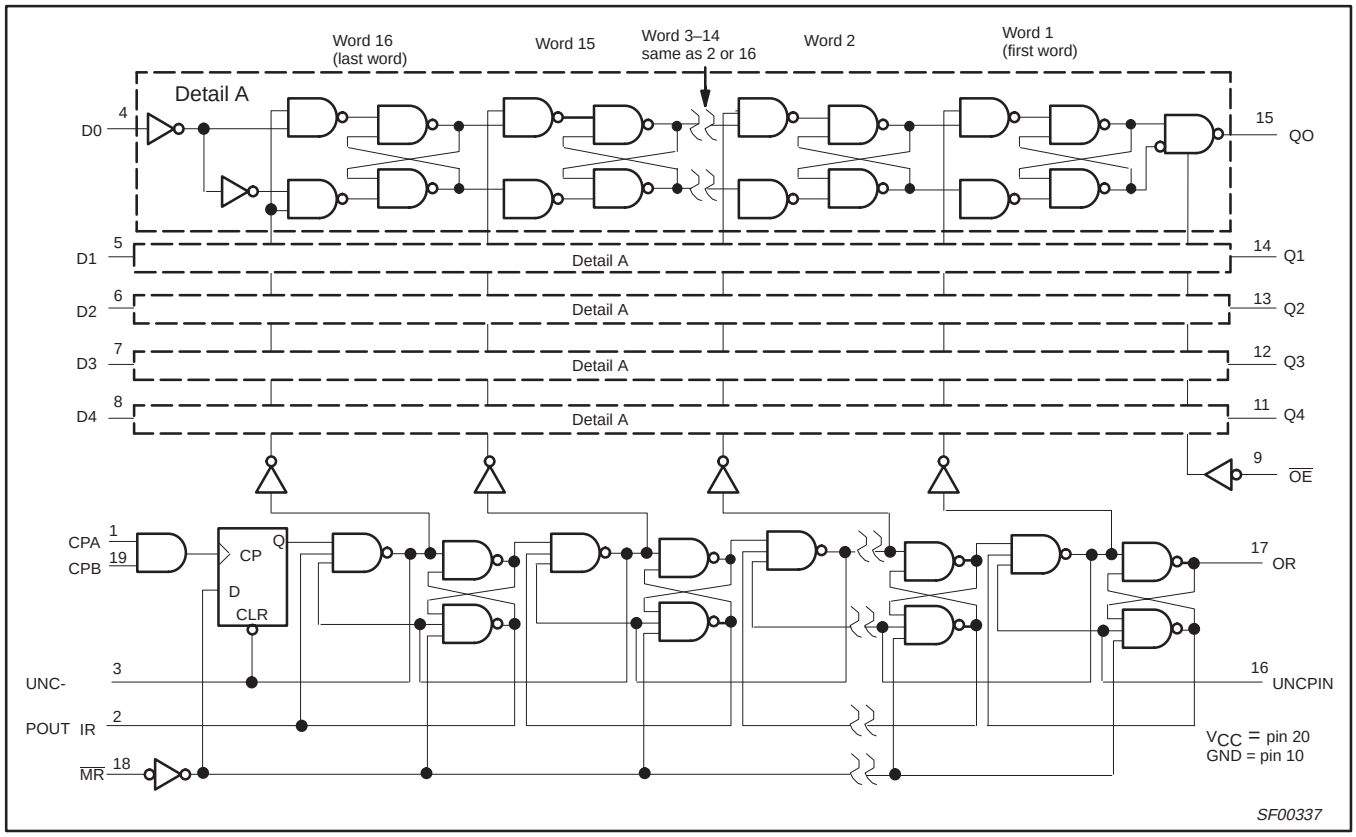
IEC/IEEE SYMBOL



LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	IR, OR, UNCPOUT	40	mA
	Current applied to output in Low output state	Data outputs	48	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	IR, OR, UNCPOUT			–1	mA
		Data outputs			–3	mA
I_{OL}	Low–level output current	IR, OR, UNCPOUT			20	mA
		Data outputs			24	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	IR, OR, UNCPOUT	V_{CC} = MIN, V_{IL} = MAX	$\pm10\%V_{CC}$	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	$\pm5\%V_{CC}$	2.7			V
		Data outputs	V_{CC} = MIN, V_{IL} = MAX	$\pm10\%V_{CC}$	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	$\pm5\%V_{CC}$	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	$\pm10\%V_{CC}$		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	$\pm5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OZH}	Offset–output current, High–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset–output current, Low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

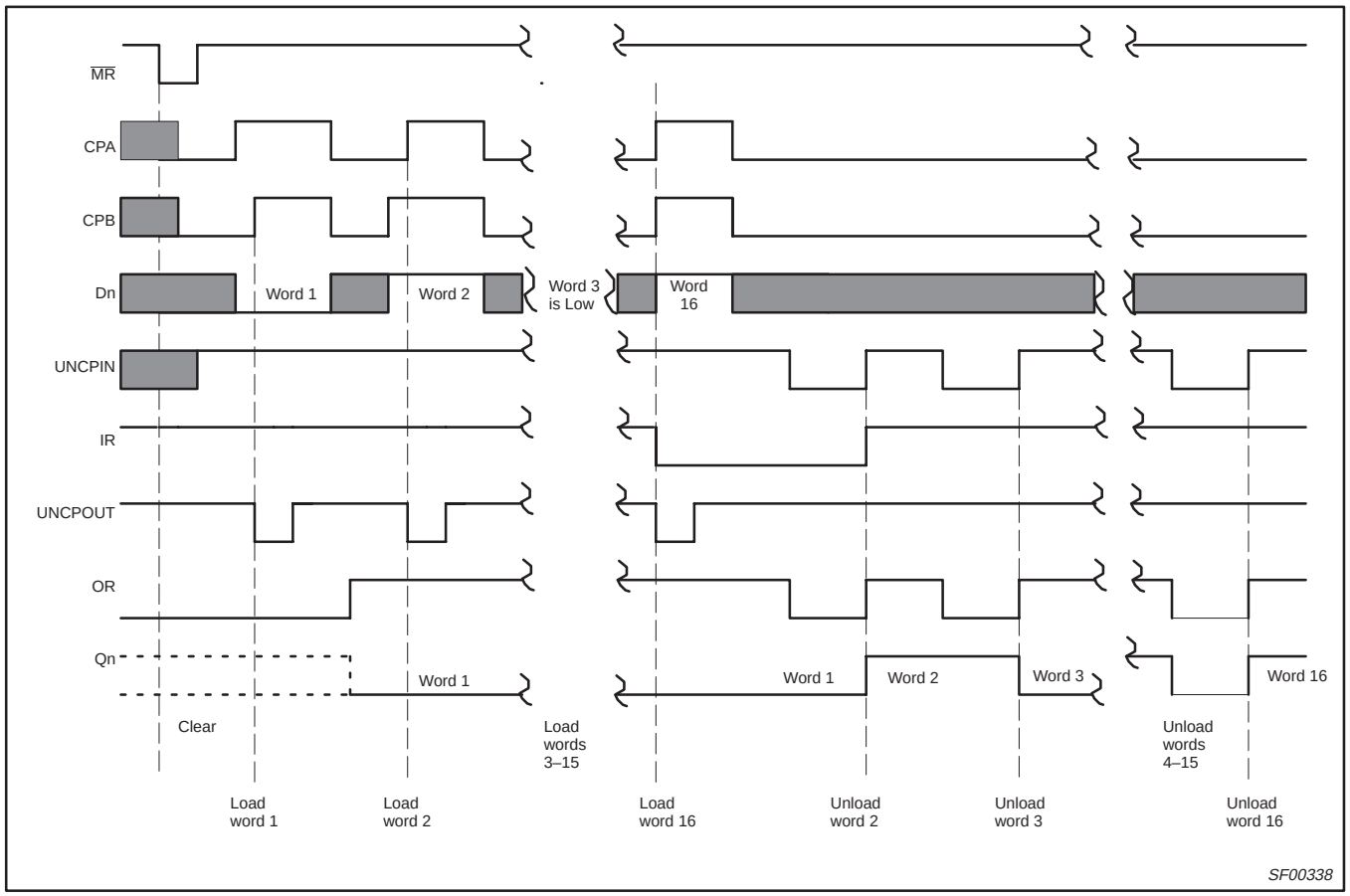
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency, Cascade mode	Waveform 2 and 3	25			25		MHz
t_{PLH} t_{PHL}	Propagation delay UNCPIN to Qn	Waveform 2	10.0 9.5	13.0 12.0	19.5 16.0	9.0 8.5	22.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay UNCPIN to OR	Waveform 2	16.0 6.0	20.0 8.5	25.0 11.0	14.0 5.0	29.0 12.0	ns
t_{SK}	Output skew Qn to OR ↑	Waveform 4	2.0		12.0	0.0	15.0	ns
t_{PLH}	Propagation delay UNCPIN to IR	Waveform 2	50	60	70	50	85	ns
t_{PLH}	Propagation delay CPA or CPB to OR	Waveform 4	55	65	75	50	90	ns
t_{PLH} t_{PHL}	Propagation delay CPA or CPB to UNCPOUT	Waveform 4	20.0 8.5	23.0 11.5	27.0 15.0	17.0 7.5	29.0 16.0	ns
t_w(L)	Pulse width, Low UNCPOUT	Waveform 4		12.0				ns
t_{PHL}	Propagation delay CPA or CPB to IR	Waveform 3	11.0	13.5	17.0	9.0	19.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to OR	Waveform 3	5.5	8.5	11.5	5.0	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to IR	Waveform 3	2.0	4.0	7.0	1.5	7.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 5 Waveform 6	1.5 2.5	3.5 4.5	6.5 7.5	1.0 2.0	7.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 5 Waveform 6	1.5 2.0	3.5 4.0	7.0 7.0	1.0 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

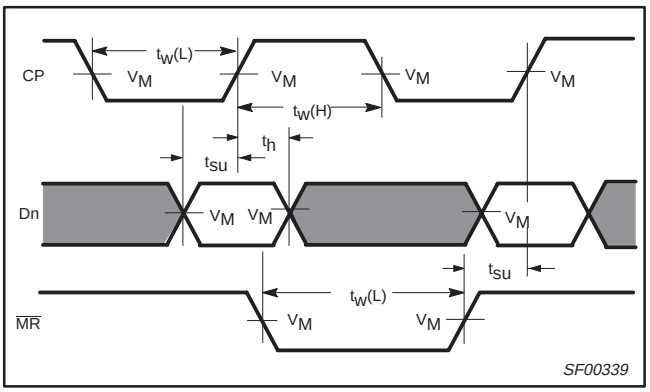
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to CPA or CPB	Waveform 1	0.0 0.0			0.0 0.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CPA or CPB	Waveform 1	14.0 12.5			16.5 14.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CPA or CPB	Waveform 1	0.0			0.0		ns
t_w(H) t_w(L)	CPA or CPB pulse width, High or Low	Waveform 1	6.5 3.0			8.5 3.5		ns
t_w(L)	UNCPIN pulse width, High or Low	Waveform 2	24.0 3.5			28.0 4.0		ns
t_w(L)	$\overline{MR}$ pulse width, Low	Waveform 1	3.5			4.5		ns

TYPICAL TIMING DIAGRAM

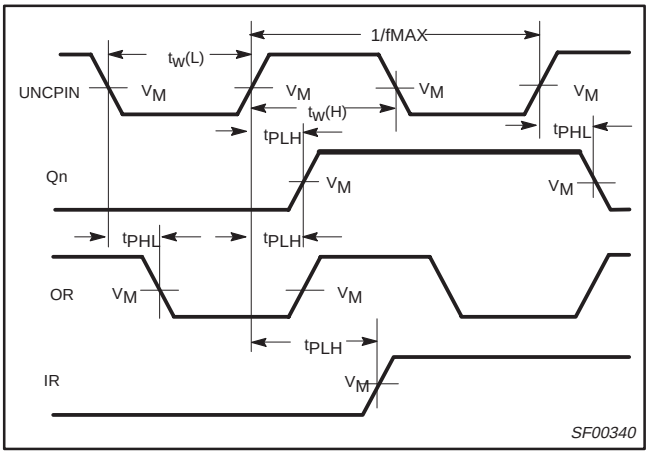


NOTE: Shaded areas Indicates irrelevant input conditions.

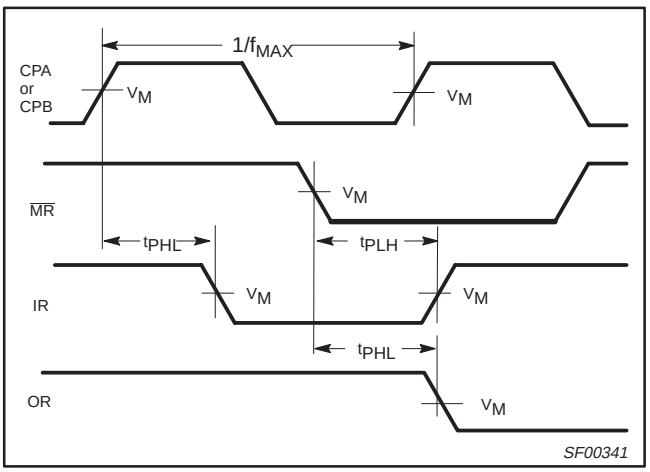
AC WAVEFORMS



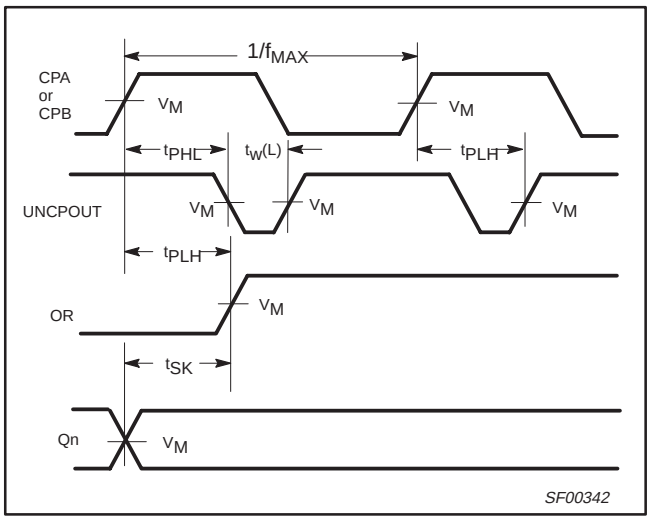
Waveform 1. $\overline{MR}$ and Clock Pulse Widths, Data Setup and Hold Times and $\overline{MR}$ to Clock Setup Time



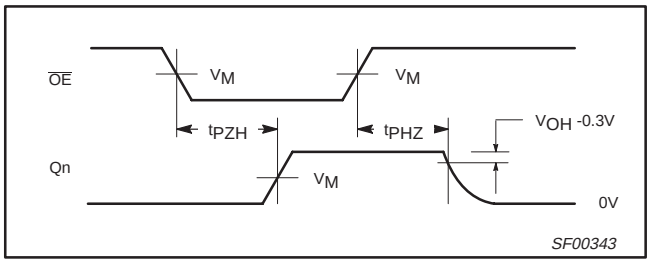
Waveform 2. UNCPIN to Output Delays



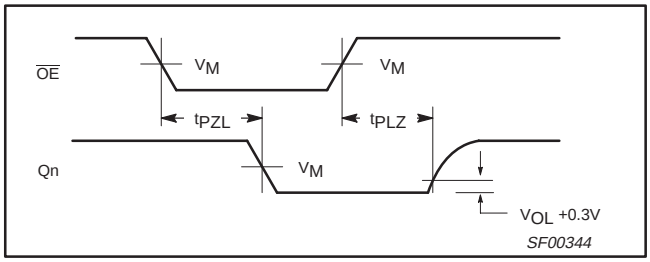
Waveform 3. CPA or CPB to IR Delay and $\overline{MR}$ to IR and OR Delay



Waveform 4. CPA or CPB to UNCPOUT and OR Delay, UNCPOUT Pulse Width and Qn to OR Skew



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION

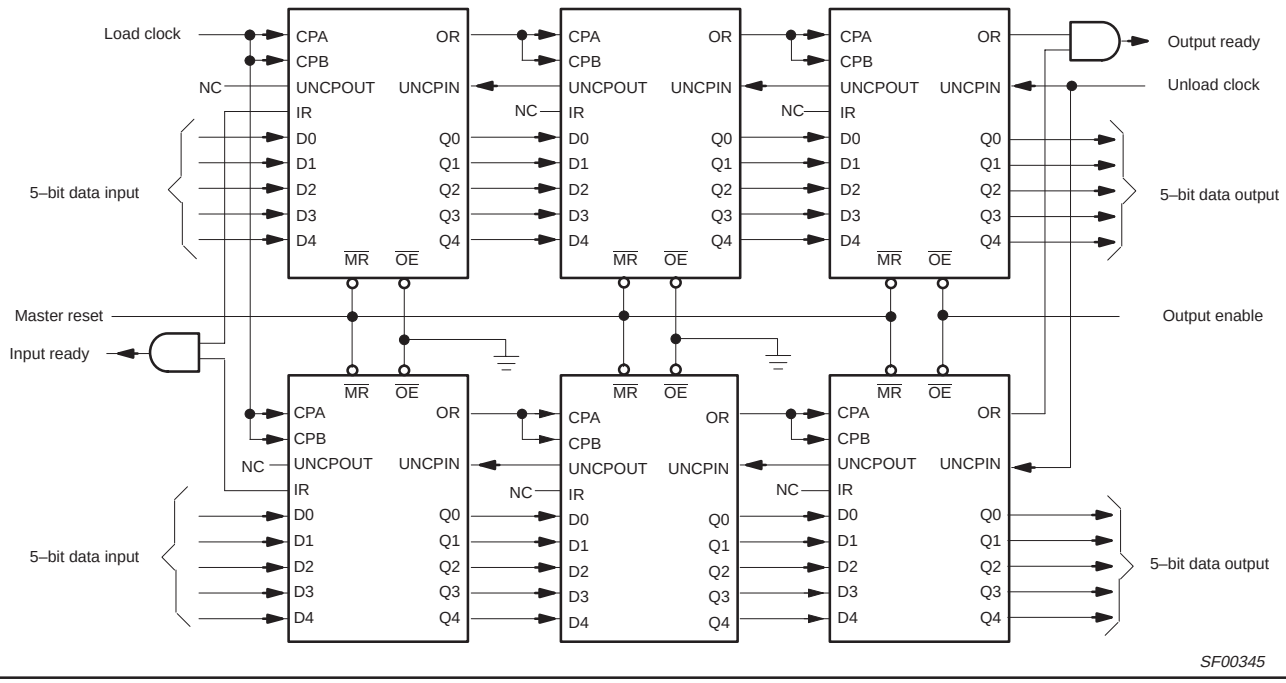
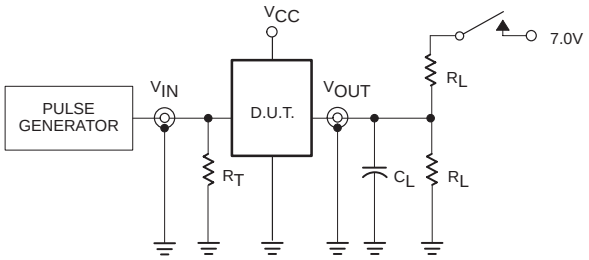


Figure 1. Expanding the 74F225 FIFO (48 words of 10 bits)

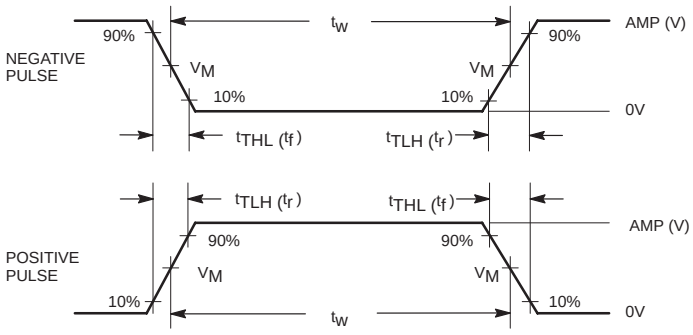
TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

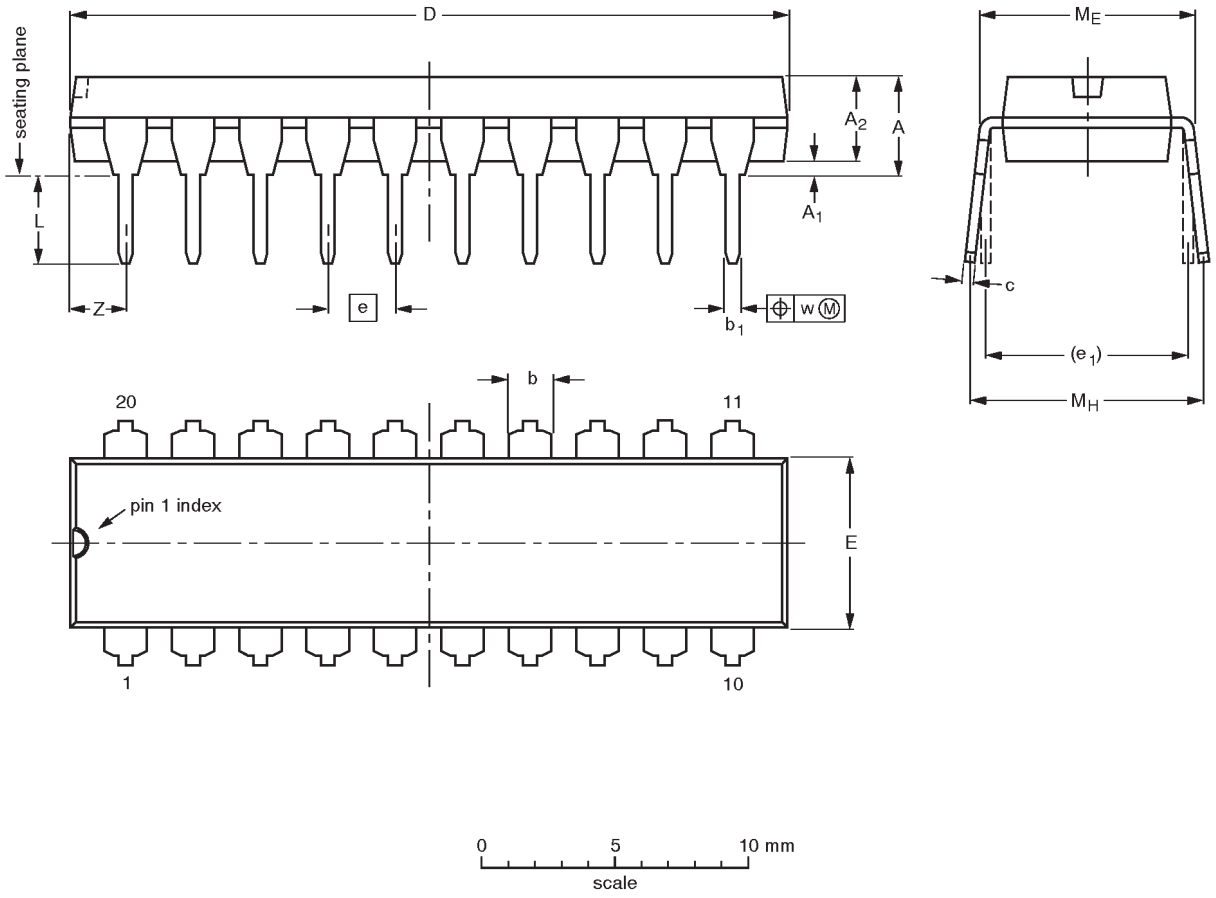
DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

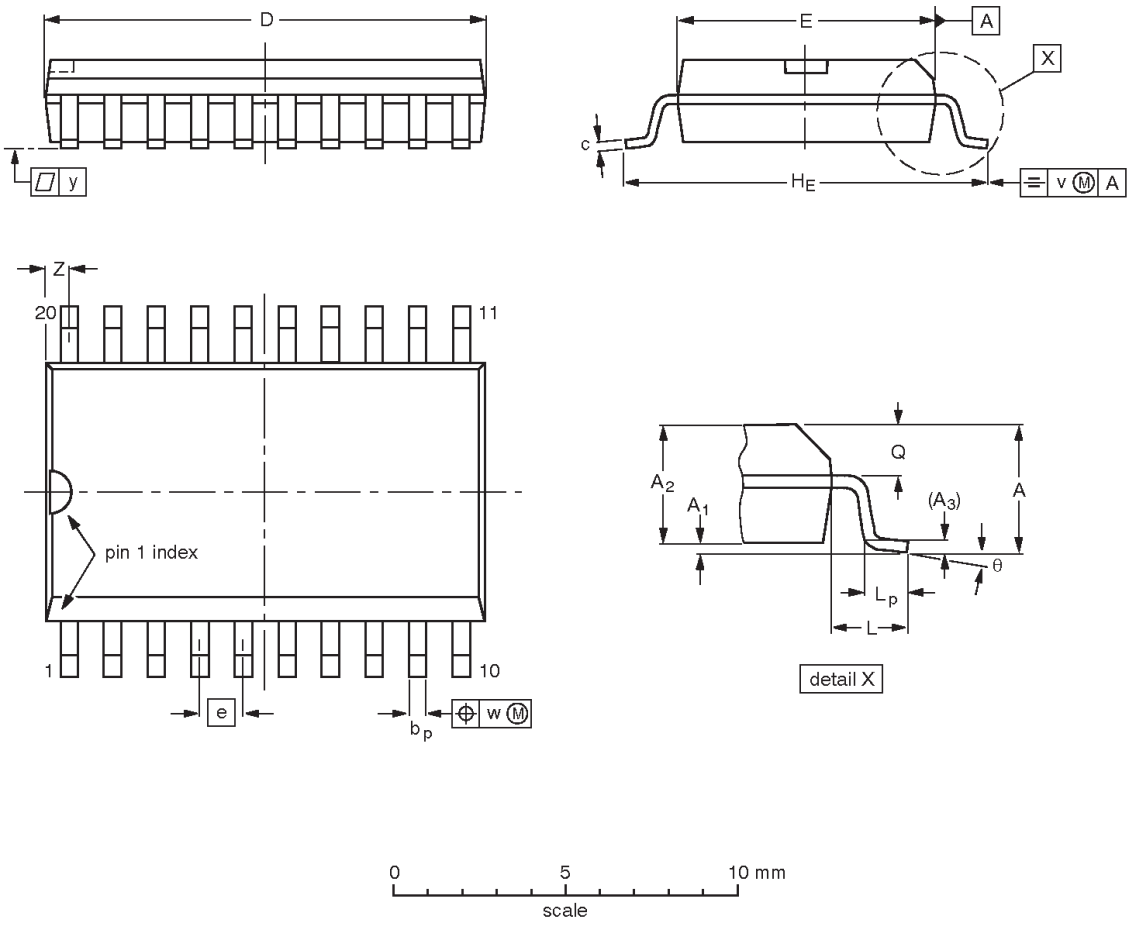
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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